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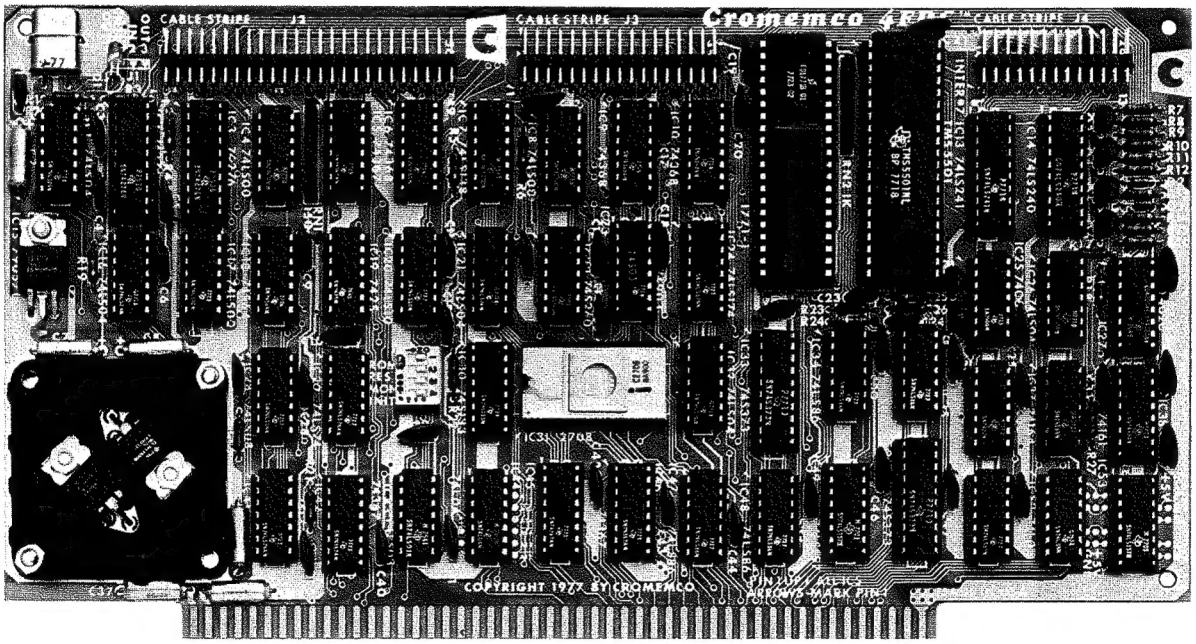
Cromemco
4FDC
Floppy Disk Controller

Instruction Manual

Cromemco

4FDC

Floppy Disk Controller



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CHAPTER 1: INTRODUCTION

The Cromemco Disk Controller (model 4FDC) is designed to interface both 5-inch ("mini") and 8-inch floppy disk drives to the S-100 computer bus used in Cromemco computers. In addition the 4FDC contains a serial I/O channel with software-selectable baud rates from 110 baud to 76,800 baud. The 4FDC controller also has a 1K resident 2708 ROM pre-programmed with Cromemco's RDOS ROM-resident Disk Operating System.

RDOS is designed to allow a operator to perform all essential disk operations from the console keyboard. RDOS also contains a bootstrap program that can be used to load the powerful Cromemco CDOS disk operating system into RAM memory from a diskette.

Four switches on the 4FDC interface card are used to set the operation of the card. Switch 1 is the RDOS DISABLE switch. When this switch is ON the 1K ROM containing RDOS cannot be accessed by the computer. When this switch is OFF the RDOS program resides in the computer memory space from address C000 to C3FF.

Switch 2 is the RDOS DISABLE AFTER BOOT switch. If this switch is ON the 1K ROM containing RDOS will automatically be disabled after CDOS is bootstrapped in from a disk thus clearing memory space from C000 to C3FF for system use. (In this mode the ROM is actually disabled by an output to port 40H which is done automatically by CDOS). If switch 2 is OFF, RDOS remains in memory space even after CDOS is loaded.

RDOS contains two programs; 1) the CDOS bootstrap program and 2) the console monitor program. Switch 3 is the BOOT ENABLE switch. When this switch is ON the bootstrap program will execute (thus loading CDOS) without first entering the monitor program. If this switch is off, RDOS begins in the console monitor mode permitting the bootstrap operation or other operations to be performed under console control.

Switch 4 is the INITIALIZATION INHIBIT switch. When this switch is ON, diskettes cannot be initialized under software control thus preventing a "runaway" program from unintentionally altering the diskette initialization. This switch must be OFF when initializing diskettes.

Both RDOS and CDOS are written to take full advantage of the Z-80 microprocessor instruction set. Complete details on RDOS are given in Chapter 2 of this manual. CDOS is described in a separate manual that is provided with Cromemco's disk software.

CHAPTER 2:

RDOS

The ROM-resident Disk Operating System has two modes of operation.

If the 4FDC board is connected to one or more disk drives equipped with the CROMEMCO CDOS operating system and DIP switch 3 is on, the monitor will boot in the operating system from the disk whenever the computer is reset.

If switch 3 is off, the monitor's command mode is accessed by resetting the computer. This mode provides control of the computer from the terminal keyboard attached to the 4FDC's serial port.

Transfer of control to a program anywhere in memory can be made from the keyboard. Commands are also included to display the contents of memory, change memory values, move and compare blocks of memory, examine input ports, write data to output ports, and change the baud rate of the serial port on the 4FDC. These commands make the 4FDC useful even without disk drives for running the computer or for debugging hardware.

There are also commands to select any of the four drives which can be attached to the 4FDC, to set its head seek rate, to seek tracks, to read or write blocks of memory to the diskette starting at any track and sector, to boot in CDOS from drive A and to change the location of the monitor's stack.

Command Format

The normal prompt of the monitor is a semi-colon, ';'. However, if a disk drive is selected the prompt changes in order to remind the user which drive is current. (See Select Disk Drive for details.)

The monitor is controlled by one and two-character commands from the terminal keyboard. The format is free-form with respect to spaces. All data is entered and printed in hexadecimal format.

In the following, DM is the Display Memory command and S is the Swath operator (See below). The four examples are equivalent commands. They display the contents of 100 hex bytes of memory beginning with location 1000 hex. ('(CR)' indicates carriage return).

```
;DM1000 10FF  (CR)
;DM1000S100  (CR)
; D M 1000 10FF  (CR)
; D M 1000 S 100 (CR)
```

When entering an address as an operand, only the last four digits typed in are retained. For example, '321000' is read as '1000'. Therefore, if a wrong digit is entered, continue typing until the last four digits are correct.

Only the last two digits typed are retained when a two-digit number such as a data byte is entered.

Swath Operator

There are two ways to specify the address range of many commands. The first is to simply list the beginning and ending addresses (and, where appropriate, the destination address). For example, the first command below displays the contents of memory between addresses E400 and E402. The second command moves (or copies) the first 1400 hex bytes of memory to memory starting at 2000 hex.

```
DM E400  E402
M 0  13FF  2000
```

Another way to do the same thing is to use the Swath operator, S, to specify the width of the address range rather than state the ending address explicitly.

```
DM E400S3
M 0  S1400  2000
```

Errors and Escapes

When the monitor detects an error condition, the command is aborted and a '?' is printed followed by the prompt ';' for the next command.

Any command may be aborted from the keyboard either when the monitor is requesting further input, or during print-out, by depressing either the ESCAPE or the ALT MODE key. CONTROL-SEMI-COLON, CONTROL-SHIFT-'K', and '}' may also work.

Baud Rates and UART Selection

When the monitor is entered, push carriage-return until the monitor responds with:

```
CROMEMCO  RDOS
```

The monitor is capable of selecting 19200, 9600, 4800, 2400, 1200, 300, 150, or 110 baud. The maximum number of carriage-returns required to select any of these baud rates is four.

The baud rate can also be changed by using Initialize command. (See below.)

Some peripheral devices such as paper tape readers or punches may have no keyboards. The baud rate can also be set by outputting a data byte from the following table to port 0.

Baud Rates	Data Byte
110	01
150	82
300	84
1200	88
2400	90
4800	A0
9600	C0

The baud rate can be octupled by outputting 10 hex to port 2. Outputting 0 to this port brings the baud rate back to normal.

System Stack

The monitor's stack normally resides in low memory between 40 and 80 hex. However, if it is in the way, it can be moved using the Kick Stack command. (see below)

Using the Monitor

Set the power-on jump switch on the ZPU card to C (1100 binary) and turn off DIP switch 3 on the 4FDC.

Depress carriage-return two to four times in order to set the UART on the 4FDC to baud rate of the terminal being used.

The monitor will then respond:

CROMEMCO RDOS

followed by a prompt ';'. The monitor is then ready to accept commands from the keyboard.

In order to boot in CDOS from drive-A simply type:

B (CR)

COMMANDS

Boot

(1) B (CR)

Boots CDOS from the diskette on drive-A. CDOS will then respond with its prompt 'A.'.

Display Memory

(2a) DM beginning-addr ending-addr (CR)

or

(2b) DM beginning-addr S swath-width

The contents of memory are displayed in hexadecimal form. Each line of the display is preceded by the address of its first byte. For example:

```
;DM100 S3
0100: C3 34 7F
```

Examine Input Port

(3) E port-number (CR)

Displays the current contents of the input port identified by port-number (in hex).

Go

(4) G starting-addr (CR)

Execution begins at starting-address.

Initialize Baud Rate

(5) I (CR)

After the carriage-return is typed, change the baud rate of the terminal to the desired value and then push carriage-return until the monitor responds with its prompt.

The monitor is capable of selecting 19200, 9600, 4800, 2400, 1200, 300, 150, or 110 baud. The maximum number of carriage returns required to select any of these baud rates is four.

Kick Stack

(6) K new-stack-location (CR)

Moves the monitor's stack from normal location at 7C hex to any convenient location in RAM memory. Remember to leave 64 (40 hex) bytes for the system stack above its new location (including 4 bytes for temporary storage above the stack proper).

Move

(7a) M source-addr source-end destination-addr (CR)

or

(7b) M source-addr S swath-width destination-addr (CR)

Move (or copy) the contents of memory beginning with source-address and ending with source-end to destination-address. After the move, the monitor verifies that source and destination are the same. This will result in a print-out of discrepancies which are not really errors after certain types of overlapping moves. However, this print-out can be terminated by depressing ESCAPE ar ALT Mode.

The move command can be used to fill a block of memory with a constant. For example, to enter zeros between locations 100 and 108, use the Substitute Memory command to enter 0 at location 100, and then move 100 through 107 to 101:

M 100 107 101

or

M 100 S 8 101

Care should be taken not to overwrite the monitor's stack which resides in low memory between 40 and 80 hex unless changed with the Kick Stack command.

Output

(8) O data-byte port-number (CR)

Writes data to the output port identified by port-number (in hex).

Read Disk

(9a) RD destination-addr destination-end sector-number (CR)

or

(9b) RD destination-addr S swath-width sector-number (CR)

Before this command will be accepted the disk drive and track number must have been specified. (See the Select Disk Drive and Seek commands below.)

Reads enough sectors from the current drive to fill the specified memory area, starting with the specified sector of the current track. Prints the first track and sector and the last track and sector read. However, if the last sector of the last track on the diskette is read before the memory area is filled then a question mark is printed and the command is terminated.

The command is also terminated if an error is read in reading a sector. In this case,a message of the following type is printed:

R-ERR nn

where nn is a hex number which indicates the status:

Bit	Indication
7	Not Ready
6	Record Type
5	Record Type
4	Record Not Found
3	CRC Error
2	Lost Data
1	Data Request
0	Busy

The number of the last track accessed can be obtained from input port 31 hex and the number of the last sector accessed from input port 32 hex. (See the Examine Input Port command.)

	Large Floppy	Mini Floppy
Tracks	0 - 4C hex	0 - 27 hex
Sectors	1 - 1A hex	1 - 12 hex

Care should be taken not to overwrite the monitor's stack which normally resides in lower RAM between 40 and 80 hex. If it is desirable to load this region of memory from the disk, first move the stack using the Kick Stack command.

Seek Track

(10) S track-number (CR)

Before this command will be accepted the disk drive must have been specified. (See the Select Disk Drive command below.)

Seeks the specified track of the current drive.

If an error is made, a message of the following type is printed:

S-ERR nn

where nn is a hex number which indicates the status:

Bit	Indication
7	Not Ready
6	Write Protect
5	Head Engaged
4	Seek Error
3	CRC Error
2	Track 0
1	Index
0	Busy

Substitute Memory

(11) SM address (CR)

Substitute Memory displays the contents of address and outputs a dot, '.', as a prompt for the substituted value. If no change is desired, type a space or another dot. Otherwise, enter the new value. The monitor accepts hex digits until it gets a delimiter, such as a space, dot, or carriage-return, retaining the last two digits entered as the value. Unless the delimiter is a carriage-return, the monitor then outputs the contents of the next sequential memory location with a dot prompt. A carriage-return terminates the command.

Verify

(12a) V source-addr source-end destination-addr (CR)

or

((12b) V source-addr S swath-width destination-addr (CR)

Verify that the block of memory between source-address and source-end contains the same values as the block beginning at destination-address. The addresses and contents are printed for each discrepancy found (unless the print-out is terminated by ESCAPE or ALT MODE)

This command works by reading bytes from the source and destination and comparing them. If a discrepancy is found, the memory is read again for print-out. Thus it can happen that a discrepancy is printed-out with the source and destination contents indicated to be the same. This is caused by a defective memory element.

Write Disk

(13a) WD source -addr source -end sector-number (CR)

or

(13b) WD source S swath-width sector-number (CR)

Before this command will be accepted the disk drive and track number must have been specified. (See the Select Disk Drive and Seek commands on previous page.)

Writes the contents of the specified memory area to the current drive, starting with the specified sector of the current track.

Prints the first track and sector and the last track and sector written. However, if part of the memory area remains after the last sector of the last track is written, a question mark is printed and the command is terminated.

The command is also terminated if an error is made in writing a sector. In this case, a message of the following type is made:

W-ERR nn

where nn is a hex number indicating the status:

Bit	Indication
7	Not Ready
6	Write Protect
5	Write Fault
4	Record Not Found
3	CRC Error
2	Lost Data
1	Data Request
0	Busy

The last track accessed can be obtained from port 31 hex. The last sector accessed from port 32 hex. (See Examine Input command.)

	Large Floppy	Mini Floppy
Tracks	0 - 4C hex	0 - 27 hex
Sectors	1 - 1A hex	1 - 12 hex

Select Disk Drive

The 4FDC will control up to four disk drives, labelled "A", "B", "C", and "D". It can handle seek speeds from the slow seek appropriate to the mini floppy to the fast seek of Cromemco's large floppy. It can also handle the medium seek of some other large floppies. To select a drive and a seek speed, type the drive label followed by one semi-colon for the fast seek, and two semi-colons for medium seek, or three semi-colons for slow seek. For example, to select drive C with slow seek, type:

C;;; (CR)

To select drive A with fast seek, type:

A; (CR)

Until the drive selection is changed the normal monitor prompt, ';', will be replaced by the disk label and speed indicator as typed, 'C;;;' in the first example.

All disk commands (Seek, Read Disk, and Write Disk) refer to the drive most recently selected.

Disk selection also restores the disk drive head to home, track 0. If an error is made in doing this a message of the following type is printed:

H-ERR nn

where nn is a hex number indicating the status:

Bit	Indication
7	Not Ready
6	Write Protect
5	Head Engaged
4	Seek Error
3	CRC Error
2	Track 0
1	Index
0	Busy

CHAPTER 3: REGISTER DESCRIPTION

The registers of the 4FDC will be discussed in numerical order according to their I/O address assignment shown below:

I/O Address (hex)	INPUT	OUTPUT
00	UART status	UART baud rate
01	UART data	UART data
02	not assigned	UART command
03	interrupt address	interrupt mask
04	parallel input	parallel out/auxiliary disk command
05	not assigned	timer 1
06	" "	timer 2
07	" "	timer 3
08	" "	timer 4
09	" "	timer 5
30	DISK status	DISK command
31	DISK track	DISK track
32	DISK sector	DISK sector
33	DISK data	DISK data
34	DISK flags	DISK control
40	not assigned	bank select

00 IN Status Register: Bit assignment by PC board traces.

D7	D6	D5	D4	D3	D2	D1	D0
Transmit Buffer Empty	Read Data Avail.	Int. Pend-ing	Start Bit Detect	Full Bit Detect	Ser-ial Rcv.	Over-Run Error	Frame Error

The functions of these flags are indicated in the following sections.

D7 Transmitter Buffer Empty (TBE):

A high in bit 7 indicates that the transmitter data buffer is ready to accept a new byte. TBE goes high as soon as the serial transmitter begins to send the byte currently in the buffer. Since the transmitter is "double-buffered", the user may respond to the TBE signal and load the buffer

even before the previous byte has been totally transmitted. TBE also activates interrupt request 5. TBE is cleared when the buffer is loaded and is set by the RESET command.

D6 Receiver Data Available (RDA):

A high in bit 6 indicates that a byte of data is available from the receiver buffer. This flag remains high until the buffer is read. A RESET command clears the flag. If the buffer is not read by the time the next byte from the receiver is ready, the new byte will write over the old byte and the overrun error flag will be set. RDA also activates interrupt request 4.

D5 Interrupt Pending (IPG):

A high in bit 5 indicates that one or more of the eight interrupt request sources has become active. This flag goes high at the same time as the interrupt request pin of the TMS 5501 UART.

D4 Start Bit Detect (SBD):

A high in bit 4 indicates that the serial receiver has detected a start bit. This bit remains high until the full character has been received. SBD is cleared by RESET command. This bit is provided for test purposes.

D3 Full Bit Detect (FBD):

The FBD flag in bit 3 goes high one full bit time after the start bit has been detected. This bit remains high until the full character has been received. FBD is cleared by a RESET command. This bit is provided for test purposes.

D2 Serial Receive (SRV):

A high in bit 2 indicates high level on the serial data input line. A low in bit 2 indicates a low level on the serial data input line. SRV is high when no data is being received. This bit is provided for break detection and for test purposes.

D1 Overrun Error (ORE):

A high in bit 1 indicates that the receiver has loaded the receiver data buffer before the previous contents were

read. ORE is cleared after the status port is read or by the RESET command.

D0 Frame Error (FME):

A high in bit 0 indicates an error in one or both of the stop bits which "framed" the last received data byte. FME remains high until a valid character is received.

00 OUT Baud Rate Register: Loading this register sets the baud rate and stop bits for serial receive and transmit data. Bit assignment is as follows:

D7	D6	D5	D4	D3	D2	D1	D0
STOP BITS	9600	4800	2400	1200	300	150	110

D7 STOP

A high in bit 7 selects one stop bit for serial receive and transmit data. A low in bit 7 selects two stop bits.

D6-D0 BAUD RATE

A high in one of the lower seven bits selects the corresponding baud rate. If more than one bit is high, the highest rate selected will result. If none of the bits are high, the serial transmitter and receiver will be disabled. (For special purposes, these baud rates can be octupled -- see the description of HBD in the command register).

01 IN Receiver Data: This register contains an assembled byte of data from the serial receiver.

01 OUT Transmitter Data: This register is loaded with data for the serial transmitter.

02 IN Not Assigned: Reading this port causes no response from the 4FDC. This address is available for other parts of the computer system.

02 OUT Command Register: The format for the command register is shown as follows:

------- latched ----------

D7	D6	D5	D4	D3	D2	D1	D0
Not Used	Not Used	Test	HIGH BAUD	INTA Enable	RST7 Sel.	Break	Reset

D5 Test Bit (TB5):

A high in bit 5 disables the internal interrupt priority logic and then enables the internal clock. Thus, the signal on the INT pin of the 5501 becomes a TTL level clock of 1562.5 Hz (12.5 kHz if HBD is high -- see D4 High Baud below). TB5 should be low for normal operation.

D4 High Baud (HBD):

A high in bit 4 octuples the rate of the internal clock. This causes the interval timers to count eight times faster and the serial data rates to increase eight-fold. When bit 4 is high, baud rates up to 76.8k are available for high speed data transfers.

D3 INTA Enable (INE):

A high in bit 3 allows the 5501 to respond to an Interrupt Acknowledge by gating a Restart instruction into the data bus at the correct time and resetting its internal interrupt request latch.

A low in bit 3 prevents the 5501 from detecting an INTA cycle. Bit 3 should be high for normal operation.

D2 RST7 Select (RS7):

A high in bit 2 connects the MSB of the parallel input port to the interrupt request latch for the lowest priority interrupt (interrupt 7). A low-to-high transition on the MSB of the parallel input port (PI7) will activate the interrupt request latch. The 4FDC provides an optional jumper to connect DRQ from the disk to PI7. This jumper is labelled "INTER 7". When the jumper is inserted and RS7 is high, DRQ's from the disk will generate interrupts.

A low in bit 2 connects the output of Timer 5 to the interrupt request latch for the lowest priority interrupt (interrupt 7). When the timer count reaches zero, the interrupt request latch will be activated.

D1 Break (BRK):

A high in bit 1 holds the serial transmitter output in the low state (spacing). RES will override (see D0 Reset below).

A low in bit 1 allows normal operation. BRK should be low for normal operation.

D0 Reset (RES):

A high in bit 0 causes the following actions:

a) The Serial Receiver goes into search mode; RDA, SBD, FBD, and ORE are set to zero. The contents of the receiver buffer are not affected.

b) The Serial Transmitter output is set high (marking). If D0 and D1 are both high, the RES function will override. RES sets TBE high.

c) The interrupt register is cleared except for the TBE interrupt request which is set high.

d) The interval timers are cleared. RES is not latched.

03 IN Interrupt Address: This register contains the encoded address of the highest priority interrupt currently requesting service. This address is identical to the "Restart" instruction op-code for the interrupt acknowledge. Thus, the register contents may be (in order of service priority):

HEX	SOURCE
C7 ---	Timer 1
CF ---	Timer 2
D7 ---	End of job (From disk)
DF ---	Timer 3
E7 ---	Receiver Data Available
EF ---	Transmitter Buffer Empty
F7 ---	Timer 4
FF ---	Timer 5 or (DRQ From Disk)

This register is provided for servicing interrupts via polling. After the register is read, the corresponding bit in the interrupt request register is reset. If the register is read when no interrupt is pending, it will read 0FFH.

03 OUT Interrupt Mask: The contents of this register are logically "And"-ed with output from the interrupt request register on the 5501. A high bit in the interrupt mask allows the corresponding request to pass on into the priority encoder. A low bit in the interrupt mask inhibits the corresponding interrupt from passing any further. Since the interrupt requests are latched independently of the state of the mask, an interrupt may be requested while the mask bit is low. The request will be retained until the mask is changed and the request allowed to pass on (assuming no RES command in the interim). The mask bit assignments are:

D7	D6	D5	D4	D3	D2	D1	D0
Timer 5	Timer 4	TBE	RDA	Timer 3	EOJ	Timer 2	Timer 1

DRQ

04 IN Parallel Input: This register contains the data presented at J4. Two bits are reserved for the 4FDC.

D7	D6	D5	D4	D3	D2	D1	D0
DRQ	SEEK IN PROGRESS	X	X	X	X	X	X

D7-DRQ (jumper option)

A high in bit seven indicates the DISK data register, PORT 33H, is requesting service. This signal is also available at ports 30H and 34H. DRQ is provided at bit seven of port 04 so that the RS7 mode of the UART may be selected (see description of RS7; bit 2 of port 2) if interrupt driven disk routines are required. When shipped, the 4FDC does not have the enabling jumper inserted. In order to use D7 as described here, insert jumper "INTER 7" just below J4.

D6 - SEEK IN PROGRESS

A high in bit six indicates the voice coil motor in the currently selected drive is in motion.

A low in bit six indicates the voice coil motor has stopped moving in the currently selected drive.

This signal is only meaningful when the currently selected drive has a voice-coil head stepper motor (e.g. PERSCI 277). In all other cases, it will float high through the 150 ohm pullup to +5 volts.

D5-D0 unassigned

The bottom six input bits are free for system use. The input data must stabilize within 75 ns after Input Strobe/ goes low and remain stable until Input Strobe/ goes high again.

04 OUT Parallel Output/Auxiliary Disk Command: This register contains the data which drives the parallel output buffers. Data is stable after Output Strobe/ rises.

D7	D6	D5	D4	D3	D2	D1	D0
X	-EJ. LEFT	-EJ. RIGHT	-FAST SEEK	-RESTORE	-CONTROL OUT	X	X
←——— PERSCI 277 OPTIONS ———→							

D7 -Not assigned

D6 -EJECT LEFT

A one in bit six causes no action. A zero in bit six activates the eject left line of J2. This bit only affects PerSci 277 drives with remote eject option. This bit is normally high.

D5 -EJECT RIGHT

A one in bit five causes no action. A zero in bit five activates the eject right line of J2. This bit only affects PerSci 277 drives with remote eject option. This bit is normally high.

D4 -FAST SEEK

A one in bit four causes no action. A zero in bit four puts the FD 1771 into fast step mode as

needed by voice coil drives. D4 should be returned to logic 1 after the drive has signalled seek complete. This bit is normally high.

D3 -RESTORE

A one in bit four causes no action. A zero in bit four causes the currently selected drive to return to Track 00. This bit is normally high.

D2 -CONTROL OUT

A high in bit 2 causes no action. A low in bit 2 pulls down pin 1 of J1 the priority Daisy-Chain. This bit is normally high.

D1,D0-Not assigned

05 IN Not Connected: Addressing this port causes no response from the 4FDC. This address is available for use by other parts of the computer system.

05 OUT Timer 1: This register contains the count used to start Timer 1. This count is decremented by 1 every 64 µseconds after initial loading. When the count reaches zero, bit 0 of the interrupt request register is set and the timer disabled. Since the maximum count is 255, the longest interval is 255x64 µseconds = 16.32 mseconds. Accuracy is plus 0 and minus 64 µseconds. Loading a count of zero causes an immediate interrupt request to the interrupt request register. Loading a new count while the timer is counting reinitializes the timer without an interrupt request. If HBD is high in the command register, the timers will count eight times as fast.

06 IN Not Connected: Same as Input 05.

06 OUT Timer 2: Operates in the same fashion as timer 1.

07 IN Not Connected: Same as Input 05.

07 OUT Timer 3: Operates in the same fashion as timer 1.

08 IN Not Connected: Same as Input 05.

08 OUT Timer 4: Operates in the same fashion as timer 1.

09 IN Not Connected: Same as Input 05.

09 OUT Timer 5: Operates in the same fashion as timer 1

30 IN Disk Status: This register's bit assignment varies according to the last command loaded into the disk command port. There are six possible assignments:

Last Command	D7	D6	D5	D4	D3	D2	D1	D0
SEEK, STEP, or RESTORE	Not Ready	Write Protect	Head Down	Not Found	CRC Error	TK 00	Index	Busy
READ RECORD(S)	Not Ready	Record Type	Record Type	Not Found	CRC Error	Lost Data	DRQ	Busy
WRITE RECORD(S)	Not Ready	Write Protect	Write Fault	Not Found	CRC Error	Lost Data	DRQ	Busy
READ ADDRESS	Not Ready	0	0	Not Found	CRC Error	Lost Data	DRQ	Busy
READ TRACK	Not Ready	0	0	0	0	Lost Data	DRQ	Busy
WRITE TRACK	Not Ready	Protect	Write Fault	0	0	Lost Data	DRQ	Busy

D7 -NOT READY

A one in bit 7 indicates the drive is unable to execute the command (e.g., the door is open). This bit is an inverted copy of the signal from the currently selected drive.

D6 -WRITE PROTECT OR RECORD TYPE

During READ RECORD(S) this bit represents bit 1, inverted, of the DATA ADDRESS MARK data byte.

During WRITE or head moving operations, this bit is set to one if the diskette in the currently selected drive has been write protected.

D5 — HEAD DOWN OR RECORD TYPE OR WRITE FAULT

During head movement commands, this bit is set to one when the head is down and the setting time has elapsed.

During READ RECORD(S), this bit represents bit 0, inverted, of the DATA ADDRESS MARK data byte.

During WRITE operations, this bit is a copy of the WRITE FAULT signal from the currently selected drive.

This bit is reset after being read.

D4 — NOT FOUND

A high in bit 4 indicates the desired track/ and or sector were not verified. During READ ADDRESS, a high in bit 4 indicates no sector address field was encountered. This bit is cleared after the status register is read.

D3 — CRC ERROR

A high in bit 3 indicates the internal CRC check did not agree with the diskette's CRC bytes. If bit 4 is set, the CRC error ocurred in an address field; otherwise, it indicates an error in a data field.

D2 — TRACK 00 OR LOST DATA

During head movement commands, a one in bit 2 indicates the head is positioned over TRACK 00 (farthest from the center). This signal is a copy of TK00 from the currently selected drive.

During data transfer commands, a one in bit 2 indicates that the computer did not respond to DRQ within one byte time (i.e., 32 µseconds or 64 µseconds for 8" or 5" drives respectively). LOST DATA is cleared after being read.

D1 – INDEX OR DRQ

During head movement commands, a one in bit 1 indicates that the diskette in the currently selected drive is passing the INDEX or beginning of the track. This bit is a copy of IP from the drive.

During READ commands, a high in bit 2 indicates the 4FDC has a data byte from the disk ready to be read at port 33H. This bit is reset after being read.

During WRITE commands, a high in bit 2 indicates the 4FDC needs a data byte from the computer at port 33H.

This bit is reset after it is read.

D0 – BUSY

A high in bit 0 indicates the 4FDC is executing a disk command and cannot accept a new disk command yet (except a FORCE INTERRUPT command; see description of FORCE INTERRUPT).

30 OUT Disk Command Register: The bit assignment varies with each command, therefore, each command will be discussed separately.

-SUMMARY-

Command	D7	D6	D5	D4	D3	D2	D1	D0
RESTORE	0	0	0	0	1	v	r_1	r_0
SEEK	0	0	0	1	1	v	r_1	r_0
STEP	0	0	1	u	1	v	r_1	r_0
STEP IN	0	1	0	u	1	v	r_1	r_0
STEP OUT	0	1	1	u	1	v	r_1	r_0
READ RECORD(S)	1	0	0	m	b	E	0	0
WRITE RECORD(S)	1	0	1	m	b	E	a_1	a_0
READ ADDRESS	1	1	0	0	0	1	0	0
READ TRACK	1	1	1	0	0	1	0	$\bar{s}$
WRITE TRACK	1	1	1	1	0	1	0	0
FORCE INTERRUPT	1	1	0	1	I_3	I_2	I_1	I_0

Flags	=1	=0
v	Verify on last track	No verify
u	Update track register	No update
m	Multiple records	Single record
b	IBM block	Other
E	Enable head load delay	Assume head is down
s̄	No synchronization	Synchronize to Address Mark

	Fields	=0	=1	=2	=3
(8" Stepping Rate)	$r_1 r_0$	6 ms	6 ms	10 ms	20 ms
(5" Stepping Rate)		12 ms	12 ms	20 ms	40 ms
	$a_1 a_0$	FB (DATA MARK)	FA	F9	F8 (DELETED DATA)

	I_3=1	I_2=1	I_1=1	I_0=1
INTERRUPT CONDITIONS:	WHEN READY	WHEN NOT READY	INDEX	IMMEDIATE

COMMAND DESCRIPTION

RESTORE

Upon receipt of this command, the Track 00 (TR00) input is sampled. If TR00 is active low indicating the Read-Write head is positioned over track 0, the Track Register is loaded with zeroes and EOJ is set. If TR00 is not active low, stepping pulses are issued until the TR00 input is activated. At this time, the Track Register is loaded with zeroes and EOJ is set.

If the TR00 input does not go active low after 255 stepping pulses, the 4FDC terminates operation, sets EOJ, and sets the Seek error status bit. Note that the RESTORE command is executed after a RESET. A verification operation takes place if the V flag is set.

SEEK

This command assumes that the Track Register contains the track number of the current position of the Read Write head and the Data Register contains the desired track number. The 4FDC will update the Track Register and issue stepping pulses in the appropriate

direction until the contents of the Track Register are equal to the contents of the Data Register (the desired track location). A verification operation takes place if the V flag is on. EOJ is set at the completion of the command.

STEP — Upon receipt of this command, the 4FDC issues one stepping pulse to the disk drive. The stepping motor direction is the same as in the previous step command. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. If the u flag is on, the Track Register is updated. EOJ is set at the completion of the command.

STEP IN — Upon receipt of this command, the 4FDC issues one stepping pulse in the direction towards the center of the diskette. If the u flag is on, the Track Register is incremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. EOJ is set at the completion of the command.

STEP OUT — Upon receipt of this command, the 4FDC issues one stepping pulse in the direction towards track 0. If the u flag is on, the Track Register is decremented by one. After a delay determined by the r_1r_0 field, a verification takes place if the V flag is on. EOJ is set at the completion of the command.

These five commands have an optional verification flag. During verification, the first encountered ID field is read off the disk. The track address of the ID field is then compared to the Track Register; if there is a match and a valid ID CRC, the verification is complete, EOJ is set, and the BUSY status bit is reset. If there is not a match but there is valid ID CRC, EOJ is set, the Seek Error status bit (Status bit 4) is set, and the BUSY status bit is reset. If there is a match but not a valid CRC, the CRC error status bit is set (Status bit 3), and the next encountered ID field is read from the disk for the verification operation. If an ID field with a valid CRC cannot be found after two revolutions of the disk, the 4FDC terminates the operation, sets EOJ, and sets record not found in the status register.

The STEP, STEP-IN, and STEP-OUT commands contain an UPDATE flag (U). When U = 1, the Track Register is updated by one for each step. When U = 0, the Track Register is not updated.

READ RECORD(S)

Upon receipt of the Read command, the head is loaded, the BUSY status bit is set; and when an ID field is encountered that has the correct track number, correct sector number, and correct CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 28 bytes of the correct field; if not, the Record Not Found status bit is set and the operation is terminated. When the first character or byte of the data field has been shifted, DRQ is generated. When the next byte is accumulated, another DRQ is generated. When the next byte is accumulated, another DRQ is generated. If the computer has not read the previous contents of the Data Register before a new character is transferred, that character is lost and the Lost Data Status bit is set. This sequence continues until the complete data field has been inputted to the computer. If there is a CRC error at the end of the data field, the CRC error status bit is set and the command is terminated (even if it is a multiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the Status Register (Bits 5 and 6) as shown below:

Status Bit 5	Status Bit 6	Data AM (HEX)
0	0	FB
0	1	FA
1	0	F9
1	1	F8

WRITE RECORD(S)

Upon receipt of the Write command, the head is loaded and the BUSY status bit is set. When an ID field is encountered that has the correct track number, correct sector number, and correct CRC, a DRQ is generated. The 4FDC counts off 11

bytes from the CRC field and the Write Gate (WG) output is made active if the DRQ is serviced (i.e., the Data Register has been loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit is set. If the DRQ has been serviced, six bytes of zeroes are written on the disk. At this time, the Data Address Mark is then written on the disk as determined by the a_1a_0 field of the command as shown below:

a_1	a_0	DATA MARK (HEX)	CLOCK MARK (HEX)
0	0	FB	C7
0	1	FA	C7
1	0	F9	C7
1	1	F8	C7

The 4FDC then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status Bit is set and a byte of zeroes is written on the disk. The command is not terminated. After the last data byte has been written on the disk, the two-byte CRC is computed internally and written on the disk followed by one byte gap of logic ones.

The two commands READ RECORD(S) and WRITE RECORD(S) contain a (b) flag which in conjunction with the sector length field contents of the ID determines the length (number of characters) of the Data field.

For IBM 3740 compatibility, the b flag should equal 1. The numbers of bytes in the data field (sector) is then 128 x 2^n where n=0,1,2,3.

For b = 1

Sector Length Field (hex)	Number of bytes in sector (decimal)
00	128
01	256
02	512
03	1024

When the b flag equals zero, the sector length field (n) multiplied by 16 determines the number of bytes in the sector or data field as shown below:

For b = 0

Sector Length Field (hex)	Number of bytes in sector (decimal)
01	16
02	32
03	48
04	64
•	•
•	•
•	•
FF	4080
00	4096

These two commands also contain a (m) flag which determines if multiple records (sectors) are to be read or written, depending upon the command. If m = 0, a single sector is read or written and EOJ is set at the completion of the command. If m = 1, multiple records are read or written with the sector register internally updated so that an address verification can occur on the next record. The 4FDC will continue to read or write multiple records and update the sector register until the sector register exceeds the number of sectors on the track. At this point, the NOT FOUND and CRC error bits are set, and EOJ is set.

READ ADDRESS

Upon receipt of the Read Address command, the head is loaded and the BUSY status bit is set. The next encountered ID field is then read in from the disk and the six data bytes of the ID field are assembled. DRQ is generated for each byte. The six bytes of the ID field are shown below:

TRACK ADDR	ZEROES	SECTOR ADDR	SECTOR LENGTH	CRC 1	CRC 2
1	2	3	4	5	6

Although the CRC characters are transferred to the computer, the 4FDC checks for validity and the CRC error status bit is set if there is a CRC error. The Sector Address of the ID field is written into the sector register. At the end of the operation, EOJ is set and the BUSY status bit is reset.

READ TRACK

Upon receipt of the Read Track command, the head is loaded and the BUSY status bit is set. Reading starts with the leading edge of the first encountered index mark and continues until the next index pulse. As each byte is assembled, it is transferred to the Data Register and the Data Request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. If bit 0 ($\bar{S}$) of the command is a 0, the accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, EOJ is set.

WRITE TRACK

Upon receipt of the Write Track command, the head is loaded and the BUSY status bit is set. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse at which time the interrupt is activated. The Data Request is activated immediately upon receiving the command, but writing will not start until after the first byte has been loaded into the Data Register. If the Data Register has not been loaded by the time the index pulse is encountered, the operation is terminated making the device Not Busy, the Lost Data status bit is set, and EOJ is set. If a byte is not present in the Data Register when needed, a byte of zeroes is substituted. Address Marks and CRC characters are written on the disk by detecting certain data byte patterns in the outgoing data stream as shown in the table below. The CRC generator is initialized when any data byte from F8 to FE is about to be written.

CONTROL BYTES FOR INITIALIZATION

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
F7	Write CRC Char.	FF
F8	Data Addres Mark	C7
F9	Data Address Mark	C7
FA	Data Address Mark	C7

DATA PATTERN (HEX)	INTERPRETATION	CLOCK MARK (HEX)
FB	Data Address Mark	C7
FC	Index Address Mark	D7
FD	Spare	
FE	ID Address Mark	C7

The Write Track command will not excecute if SW4 is ON. Note that one F7 pattern generates 2 CRC characters.

FORCE INTERRUPT

This command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command will be terminated and EOJ will be set when the condition specified in the I_0 through I_3 field is detected. The interrupt conditions are shown below:

I_0 = Not-Ready-To-Ready Transition
I_1 = Ready-To-Not-Ready Transition
I_2 = Every Index Pulse
I_3 = Immediate Interrupt

If $I_3 - I_0 = 0$, the command will be terminated but EOJ will not be set. The FORCE INTERRUPT commands above must be cleared in this manner before the 4FDC is given its next command.

31 IN/OUT Track Register: This register holds the track number of the current Read/Write head position. It is incremented by one every time the head is stepped in (towards track 76) and decremented by one when the head is stepped out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write, and Verify operations. This register should not be loaded when the 4FDC is busy.

32 IN/OUT Sector Register: This register holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. This register should not be loaded when the device is busy.

33 IN/OUT Data Register: This register is used as a holding register during Disk Read and Write operations. In Disk Read operations, the assembled data byte is transferred in parallel to the Data Register from the Data Shift Register. In Disk Write operations, information is transferred in parallel from the Data Register to the Data Shift Register.

34 IN Disk Flags: This port provides four signals.

D7	D6	D5	D4	D3	D2	D1	D0
DRQ	$\overline{\text{BOOT}}$	HEADLOAD	X	X	X	X	EOJ

D7 -DRQ

A high in bit 7 indicates the 4FDC has a byte from the disk or needs a byte for the disk according to the current operation.

D6 -$\overline{\text{BOOT}}$

A low in bit 6 indicates that SW3 is set to BOOT.

A high in bit 6 indicates SW3 is set to MON.

D5 -HEADLOAD

A one in bit 5 indicates the head of the currently selected drive is loaded.

A zero in bit 5 indicates the head has unloaded.

D4-D1 -Unassigned

D0 -EOJ

A one in bit 0 indicates the command has finished. (End of job)

34 OUT Disk Control:

D7	D6	D5	D4	D3	D2	D1	D0
AUTO WAIT	X	MOTOR ON	MAXI	DS4	DS3	DS2	DS1

D7 -AUTO WAIT

A one in bit seven puts the 4FDC into Auto Wait mode which means that subsequent reading of Input port 34H will hold the CPU in a WAIT state until one of three things happen:

a) The 4FDC issues a DRQ (this is the normal use of AUTO WAIT).

b) The 4FDC issues EOJ - this terminates the AUTO WAIT condition (the normal method of termination).

c) There is a hardware RESET.

D6 -Unassigned

D5 -Motor On

A one in bit 5 activates the motor-on signal to all disk drives.

A zero in bit 5 deactivates the motor- on signal to all disk drives.

This bit is set by RESET.

D4 -MAXI

A one in bit 4 conditions the 4FDC for an 8" disk drive.

A zero in bit 4 conditions the 4FDC for a 5" disk drive (Mini).

This bit is set by RESET.

D3-D0 -DRIVE SELECT

A high in bits 3 through 0 selects the corresponding disk drive for all further operations. Only one drive should be selected at a given time. RESET deselects all drives.

40 OUT Bank Select: Outputting any byte to port 40H will disable the 1K ROM on the 4FDC if SW2 is on. The ROM may be re-enabled by RESET.

CHAPTER 4: INTERFACE CHARACTERISTICS - S-100

The 4FDC appears on the S-100 bus as a 1K memory card and 15 I/O ports. The 4FDC is capable of generating interrupts and responding on a prioritized basis to the interrupt acknowledge cycle. (N.B. CDOS does not use the interrupt capability of the board.) Data exchange for the disk and serial I/O is programmed, not via direct memory access (DMA). This requires a minimum CPU speed of 2 mHz and no memory wait states (at 2mHz) in the buffer memory.

The Bootstrap/Monitor ROM is addressed at C000-C3FFH. This address may be changed by cutting traces and inserting jumpers at IC44. Hold acknowledge will temporarily disable the ROM. At 4mHz, the 4FDC inserts one wait state on M1 (instruction fetch) cycles for Z80 compatibility. There are no wait states at 2mHz. When switch one is on, the ROM is defeated and the 4FDC occupies no address space in memory. When switch 2 is on, the ROM is disabled as soon as a byte (any byte) is written to output port 40H, the bank select port. The ROM is re-enabled by a hardware RESET.

The serial I/O channel requires 10 I/O addresses. CDOS requires these to start at I/O address 00, the way the 4FDC is shipped. The starting address may change at 10, 20, 50, 60, or 70 H by cutting the trace at the "0" output of IC 7 and moving it to another output pin. The serial I/O channel is asynchronous because it uses the on-board clock. When one of the serial I/O channel's ports is addressed by the CPU, the 4FDC pulls down PRDY and holds it down until the 4FDC synchronizes with the CPU (up to 1 usec.)

The disk I/O ports are synchronous. CDOS assumes a base address of 30H, although this may be changed by cutting the trace at the "3" output of IC7 as explained above. There are two cases in which the 4FDC will create wait states for the disk I/O ports: 1) if the ports 30-33H are read at 4 mHz there will be one wait state added for the FD1771 data to stabilize, and 2) if the Auto-Wait mode has been selected an indefinite number of waits will be added to read or write operations on port 34H. The CPU will stay in a WAIT state until the 4FDC issues a Data Request or an End of Job signal (or there is a hardware RESET). This mode is used when reading or writing 8" diskettes with a 2mHz CPU.

Interface Characteristics - Serial Channel

The 4FDC provides both RS-232 and 20 mA current loop interface. For RS-232 connect three wires from your terminal as follows:

4FDC* J4	RS-232 terminal (i.e. CRT)
pin 7	Signal ground (not chassis)
pin 3	Receiver data (for display)
pin 2	Transmitter data (keyboard)

Some terminals may require additional modem control signals such as Clear to Send, Data Set Ready, Data Carrier Detect, etc. These may be wired to J4 pin 23 of the 4FDC.

For 20 ma teletype interface, make the following connections:

4FDC J4	ASR33 (rear terminal block)
pin 25	terminal 6 (printer current out)
pin 24	terminal 3 (keyboard current out)
pin 23	terminal 7 (printer current in)
pin 17	terminal 4 (keyboard current in)

Interface Characteristics - 8" and 5" Disk Drives

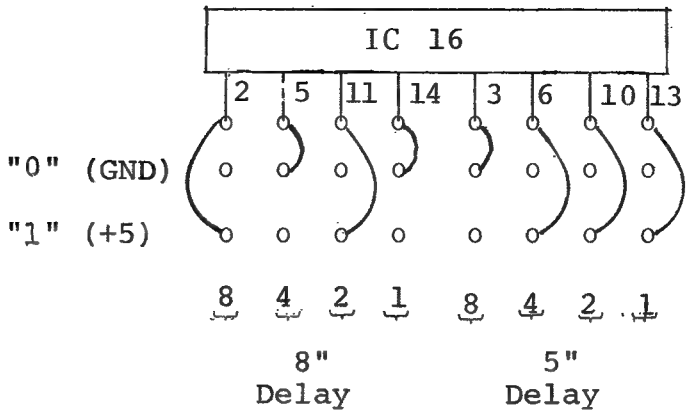
The 4FDC drives J2 and J3, the Disk Drive Signal Cable Connectors, in parallel through separate sets of TTL bus drivers. The Signal cables should be terminated (150 ohm resistors to +5 volts) at the end of the cable only. If more than one driver per cable is used, only the last drive on the cable should use pullups. Signals from the drives back to the controller are terminated on the 4FDC with 150 ohm pullups.

Outputs from the 4FDC: (all active low 0.6 volts)

DS1
DS2
DS3
DS4

These are the four drive select signals. When a drive select signal is active the selected drive should enable its data and status drivers and load the read/write head. All other drives should ignore signals until selected. When DRIVE SELECT is first asserted, the 4FDC waits a fixed amount of time for the head to LOAD before reading or writing the diskette. This time delay is 48 ms for 8" drives and 72 ms for 5" drives. The delay may be changed by rewiring IC53. The delay is 8 milliseconds times (16 - delay jumper value) as shown on the following page.

*WARNING: Connect only the three wires shown. If your cable has connections to other pins (used in some RS-232 installations) this can cause malfunction of the 4FDC interface.



STEP — This line goes active low for 16 microseconds to move the head of the selected drive in the direction specified by output DIRC. For multiple steps, the stepping rate is determined by the format of the command given to the 4FDC and will be 6, 10 or 20 milliseconds per step for large floppies (except voice coil types like the PerSci 277, in which case it is about 400 microseconds per step) or 12, 20 or 40 milliseconds per step for small floppies. The 4FDC will wait one stepping period after the last step for the Head to settle before attempting to read or write the diskette.

DIRC — When this line is asserted (low) pulses on the STEP line should cause the head of the selected drive to advance one track per step towards the center of the diskette. If DIRC is high, pulses on the STEP line should cause the head of the selected drive to retreat on track per step towards the outer edge of the diskette (towards Track 00.)

Motor On — This signal turns on the motors of all drives when low. When high it turns off the motors off all drives (so equipped).

WRITE GATE — This signal goes low to enable diskette write operations.

WRITE DATA — This signal contains the intermingled clock and data pulses to be written on the diskette. Pulse width is 500 nanoseconds for 8" drives, 1 microsecond for 5" drives.

RESTORE — This signal requests the head of the selected drive to return to TRACK 00. This signal is not used by the CDOS drivers.

EJECT LEFT — This signal requests the currently selected PerSci 277 to eject its left hand diskette.

EJECT RIGHT — This signal requests the currently selected PerSci 277 to eject its right hand diskette.

Inputs to the 4FDC (all active low 0.6 volts)

INDEX — This line should go low for at least 10 useconds once per revolution of the diskette.

TRACK 00 — This signal should go low and stay low while the selected drive is on track 00, the outermost track.

READY — This signal should be low when the disk drive is operable (i.e. door is closed, motor speed up, etc.) The 4FDC will always initiate a command regardless of the state of ready; the purpose of the signal is for detecting disk change operations using the Force Interrupt command.

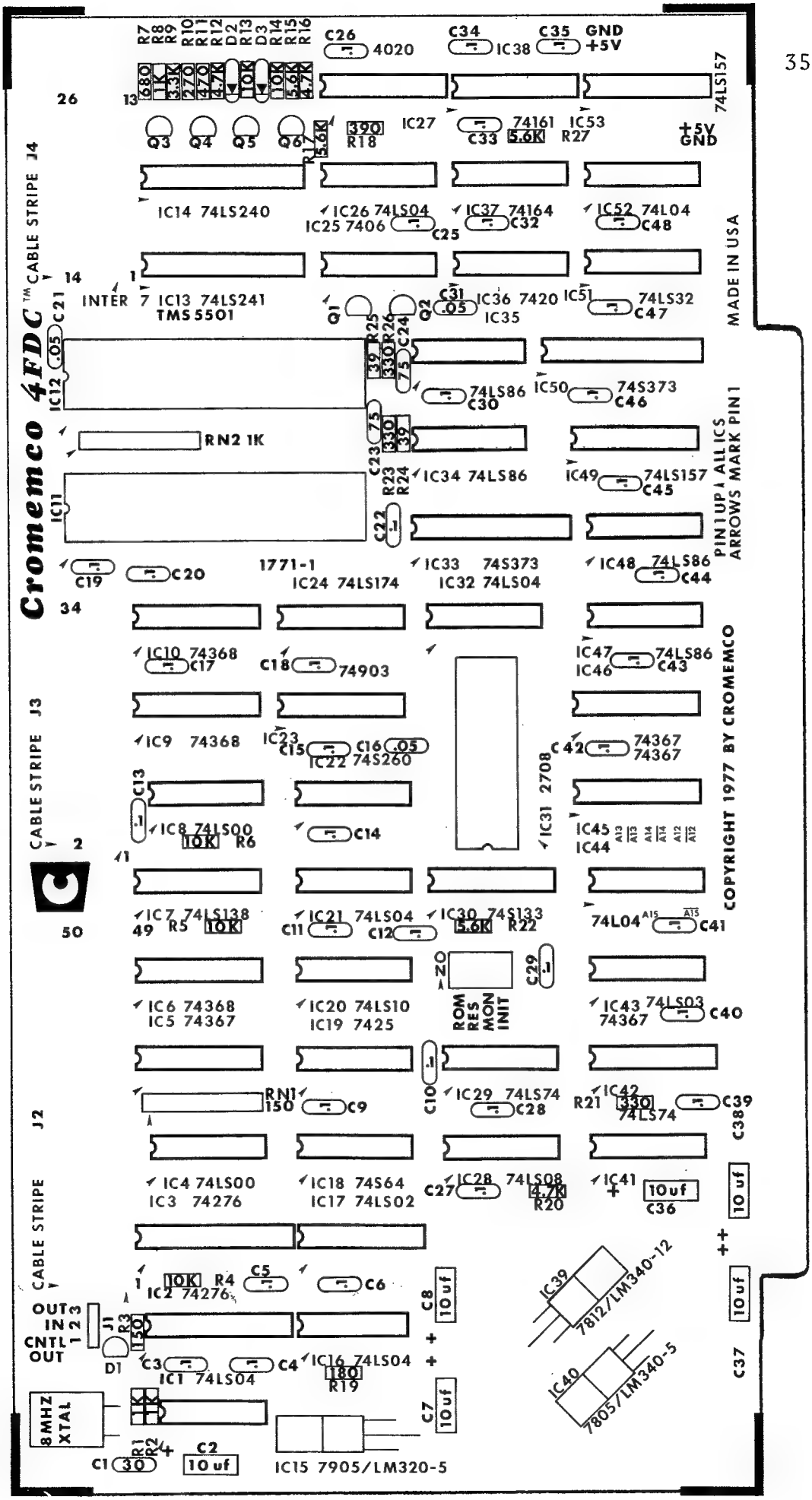
WRITE PROTECT — This signal goes low if a write-protected diskette is in the currently selected drive.

READ DATA — This signal is composite clock and data pulses from the 5" drive. The line should go low for 1 microsecond for each flux reversal on the surface of the diskette.

SEP DATA — This signal contains the data (separated from the clock pulses) from the currently selected 8" drive. The pulse should be low for 250 nanoseconds.

SEP CLK — This signal contains the clock stream (separated from the data pulses) from the currently selected 8" drive. The pulses should be active low for 250 nanoseconds.

SEEK COMPLETE — This signal should go low when the voice coil drive has positioned the read/write head over the desired track. This signal is gated with drive select and applies only to voice coil drives like the PerSci 277.


Cromemco 4FDC™
CABLE STRIPE J4
CABLE STRIPE J3
CABLE STRIPE J2
CABLE STRIPE
MADE IN USA
PIN 1 UP ALL ICS
ARROWS MARK PIN 1
COPYRIGHT 1977 BY CROMEMCO
ROM RES MON INIT
IC1 74LS04
IC2 74276
IC3 74276
IC4 74LS00
IC5 74367
IC6 74368
IC7 74LS138
IC8 74LS00
IC9 74368
IC10 74368
IC11
IC12
IC13 74LS241 TMS5501
IC14 74LS240
IC15 7905/LM320-5
IC16 74LS04
IC17 74LS02
IC18 74S64
IC19 7425
IC20 74LS10
IC21 74LS04
IC22 74S260
IC23
IC24 74LS174
IC25 7406
IC26 74LS04
IC27
IC28 74LS08
IC29 74LS74
IC30 74S133
IC31 2708
IC32 74LS04
IC33 74S373
IC34 74LS86
IC35
IC36 7420
IC37 74164
IC38
IC39 7812/LM340-12
IC40 7805/LM340-5
IC41
IC42 74LS74
IC43 74LS03
IC44
IC45
IC46
IC47 74LS86
IC48 74LS86
IC49 74LS157
IC50 74S373
IC51 74LS32
IC52 74L04
IC53 74LS157
1771-1
INTER 7
RN1 150
RN2 1K
R1 30
R2
R3 150
R4 10K
R5 10K
R6 10K
R7 680
R8 1K
R9 3.3K
R10 2700
R11 4700
R12 10K
R13 10K
R14 10K
R15 5.6K
R16 4.7K
R17 5.6K
R18 390
R19 180
R20 4.7K
R21 330
R22 5.6K
R23
R24
R25 39
R26 330
R27 5.6K
C1 30
C2 10 uf
C3
C4
C5
C6
C7 10uf
C8 10uf
C9
C10
C11
C12
C13
C14
C15
C16 .05
C17
C18 74903
C19
C20
C21 .05
C22
C23 75
C24 75
C25
C26 .1 4020
C27
C28
C29
C30 74LS86
C31 .05
C32
C33 74161
C34 .1
C35 .1 GND +5V
C36 10uf
C37 10uf
C38 10 uf
C39
C40
C41
C42 74367
C43
C44
C45
C46
C47
C48
Q1
Q2
Q3
Q4
Q5
Q6
D1
J1
OUT
IN
CNTL OUT
8 MHZ XTAL
+5V GND

CHAPTER 6: INITIAL SET-UP

4FDC Switches - For initial check-out operation set switches 1, 2, and 3 OFF and switch 4 ON. For operation after initial check-out set switches 1 OFF, and switches 2, 3, and 4 ON. The function of these switches is as follows:

	FUNCTION WHEN OFF	FUNCTION WHEN ON	SETTING FOR INITIAL CHECK-OUT	"NORMAL" SETTING
SWITCH 1	Permits monitor/ boot ROM to be read.	Totally disables monitor boot ROM.	OFF	OFF
SWITCH 2	Keeps the monitor/boot ROM Resident (by disabling the bank select).	Disables the monitor/boot ROM after the first output to I/O port 40H (bank select).	OFF	ON
SWITCH 3	Signals the monitor/boot program to stay in monitor mode.	Signals the monitor/boot program to go to the boot mode.	OFF	ON
SWITCH 4	Permits the 4FDC to initialize diskettes.	Inhibits initialization of diskettes.	ON	ON

4FDC Cables - Place the 4FDC in front of you with component side up and J1-J4 away from you. Plug in disk and terminal cables as follows:

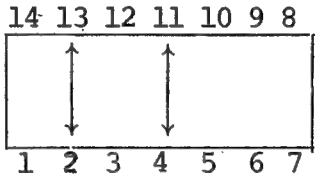
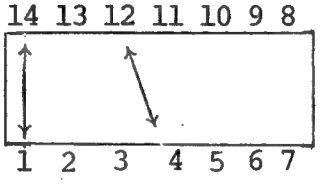
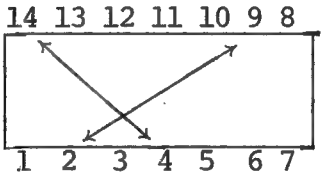
Connector	Function	Cable Size
J2	8" disk daisy chain PerSci 277	50 Conductor
J3	5" disk daisy chain (for WANGCO 82 drive)	34 Conductor
J4	Serial Interface (CRT, TTY, etc.)	26 Conductor

Be certain that the cable stripe is on the left when the cables are plugged in.

PerSci Model 277 Set-Up

Connect DC power to J3 on the PerSci drive. Connect the 50 pin cable from J2 on the 4FDC to P1 on the PerSci.

Assign drive numbers to the PerSci by wiring the 14 pin jumper inserted in U11 on the PerSci as follows:

Left Side of PerSci	Right Side of PerSci	Jumper Set-Up (top view of plug)
Drive A	Drive B	
Drive B	Drive C	
Drive C	Drive D	

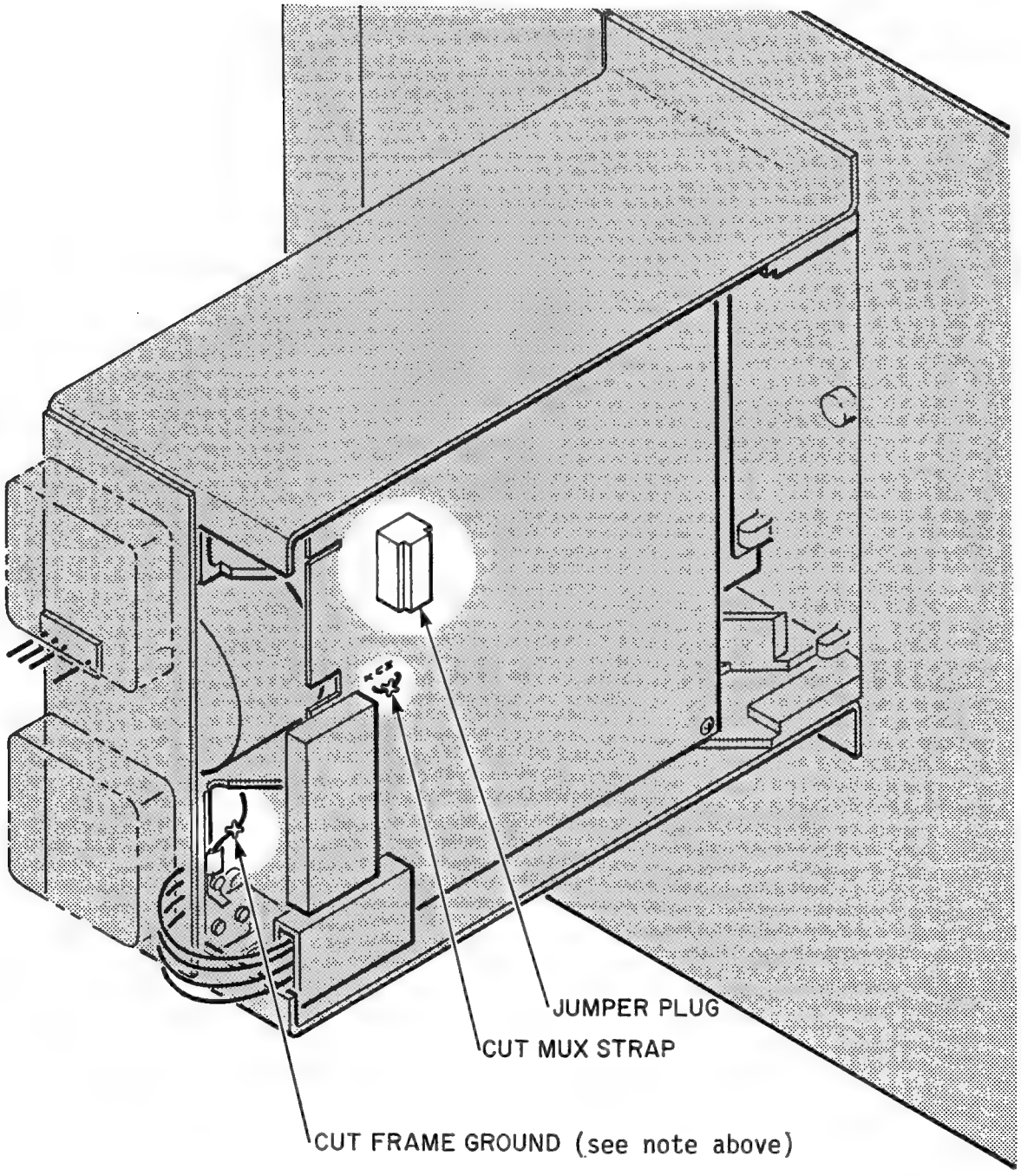
If your system uses two Model 277s,remove termination pack U1 from the drive electrically closer to the 4FDC.

WANGCO Model 82 Set-Up

Cut the jumper wire on the PC board of the Wangco Model 82 labelled "MUX" (just above J4, the big blade connector in back).

Locate the package of jumper straps just above the PC board edge connector. The first 3 jumper positions, labelled "DS1", "DS2", "DS3", select DRIVE A, DRIVE B, or DRIVE C respectively. Cut the 2 jumpers that don't apply to your configuration (or simply bend out the pins on the jumper pack so they don't contact the socket). The 5 remaining jumpers connect line terminating resistors. For single drive set-ups, these jumpers are left intact. For 2 or more drives, the jumpers are left intact on the drive at the end of the control cable only; the other drives have these jumpers cut (or bent) out.

Fig. 6-1. When using the Wangco model 82 disk drive with the Cromemco model 4FDC controller the "MUX" strap must be disconnected as shown in this figure. The jumper plug shown in the figure must be configured as described in the text. The frame ground strap must remain connected if the disk drive is a model WFD (stand-alone). It must be cut only if the disk drive is used in a Z-2D system.



Finally, locate the spade lug ground on the rear chassis with a white wire under it. Remove the spade lug, disconnect the white wire, and replace the spade lug. Tape the white wire (or cut it off); it is no longer needed. This isolates chassis ground from logic ground. (See Figure 6-1 for details).

Initial Check-Out

Set the MON switch 3, to the MON position (off); the RESident switch, switch 2, to RES position (off); and the ROM enable switch to ROM position (off). Verify that your computer has a processor and at least 1K of read/write memory addressed anywhere but C000 (the Monitor/Boot coldstart entry point).

Since the MON switch is selected. the Monitor program will be excuted instead of the Bootstrap loader. Press "Carriage Return" on your terminal until the monitor signon message appears, indicating that the monitor has successfully determined the terminals baud rate. Legal Baud rates are 110, 150, 300, 1200, 2400, 4800, 9600, and 19,200.

Insert a diskette in your Drive A and verify the drive performance by calibrating the drive, seeking out 2 tracks, and reading the first sector as detailed below:

```
          ;A;  This restores the head if 8"; type A;;; for 5"drive
        A;S2   Seek track 2
A;RD 80 S 80 1 Reads into 80H the last sector
```

To bring up the Cromemco Disk Operating System, set up your computer with 32 kilobytes of read/write memory addressed from 0000-7FFFH. This memory must be full speed (450 ns acess time maximum) if you are running an 8" disk drive and have a 2mHz processor. We recommend either the 4KZ static memory or 16KZ dynamic memory cards for reliable operation at both 2 and 4 mHz. If you have a Cromemco ZPU, set it for 2 or 4 mHz operation as desired (CPU speed does not affect disk performance) and set the power-on-jump address to "C000" (i.e. A15=A14=1). On the 4FDC set the MON switch, switch 3, to the BOOT position (on) and the RESident switch, switch 2, to the BANK position (on).

Power up the system and execute C000 H. The head will load on drive A as the Bootstrap program in the ROM reads in sector 1 of track 00, and transfers program control to CDOS, and "deboots" (the ROM disables itself, leaving address C000-C3FFH free for the system if necessary). Press "Carriage Return" on your terminal until the CDOS signon message appears, indicating that CDOS has successfully determined the terminal's baud rate. The head will load again as more of the CDOS program is read into memory. The command DIR will list the names of the files on the disk.

CHAPTER 7: THEORY OF OPERATION

Power Supplies

The unregulated bus power lines are converted to regulated supplies of +5, -5, and +12 volts by ICs 40, 15, and 39 respectively. The 4FDC requires 1.0 A at +8 unregulated, 0.100 A at +18 unregulated, and 0.100 A at -18 unregulated.

Address Decode

The 4FDC decodes address and status signals on the bus to find the following conditions: 1) Memory read cycles in the address range C000-C3FFH, 2) Input/Output references in the address range 00-09, 3) Input/Output references in the address range 30-34H, and 4) Output references to port 40H.

In case 1, IC30P9 will go low, enabling the 1K prom IC31.

In case 2, the address decoding is done in two stages. First, the base address is decoded by IC7, then the offset is determined by IC23. Pin 15 of IC7 goes low for addresses in the range of 00-0FH.

In case 3, IC7P12 goes low when the address base 30-3FH is detected. Further decoding is performed by IC11's address inputs and by the gating in the read/write circuits of IC36. Input or output references to port 34H are signalled by a high level at IC22P5.

In case 4, IC7P11 goes low for address base 40-4FH. IC8P11 goes low for outputs with an offset of 0, thus clocking IC29 on output references to port 40H.

Data Bus

The 4FDC has a three state, bidirectional internal data bus. It is coupled to the Data In and Data Out buses on the S-100 bus through latch ICs 33 and 50. There are four cases of operation determined by the particular 4FDC function being addressed.

Case 1, Memory Read: When IC30P9 goes low selecting the 2708, data appears at the inputs of exclusive-or gates ICs 34 and 35. The common input to these gates is held low by a signal from IC7, so data passes through the ex-ors without being inverted. Next, four bits are presented to multiplexer IC49. The select pin IC49P1 is held high by a signal from IC23, so data passes straight through the multiplexer. Eight bits of data now are presented to the latch IC50. The gate of the latch, IC50P11, is held high by IC20P8 as long as the ROM is enabled, so data passes through the latch. The three-state output drivers of the latch are enabled during PDBIN by a low at IC19P6.

Case 2, Input/Output references in the range 00-09H: When the TMS5501 IC12 is addressed, the 4FDC emulates an 8080 I/O cycle (M3). This is necessary to generate strobed status bits and to insure the correct read/write timing. The cycle begins when IC23P5 goes low presenting a high to the JK inputs of the first section of IC3. This section of IC3 is clocked by the falling edge of internal 02 and shifts a high level to IC3P2. This high level generates an internal SYNC pulse at IC17P13. The internal SYNC pulse enables status strobe drivers IC43P8 and IC43P11 (Write Output and Interrupt Acknowledge respectively), disables the incoming bus drivers on IC33 and triggers the SYNC pin of the TMS5501. SYNC is terminated by the rising edge of 02 which clocks the next section of IC3 and presents a high level at IC3P12. During this period, the TMS5501 internally arranges data paths while the 4FDC idles. When 02 falls again, IC20P6 goes low which opens the gate of the output latch IC50 admitting the data present at the inputs of IC30. This data has come from the TMS5501 via exclusive-or gates IC34 and IC35 and multiplexer IC49. The exclusive-ors have a common input held low by an output from IC7, so they pass the data through without inversion. Multiplixer IC49 passes the data straight through except when the 4FDC is in the process of reading the serial status port (Input port 00). In this case, IC23P5 goes low causing the multiplexer to switch D7 and D6 with D4 and D3 (producing the status bit assignment detailed in Chapter 3). The cycle finally terminates when 02 rises again shifting a high level to IC3P16.

Case 3, Input/Output references to ports 30-34H: When IC7P12 goes low signifying disk reference operations, the common pins of exclusive-or gates ICs 34, 35, 47, and 48 go high. This causes the internal data bus of the 4FDC to be complemented with respect to the S-100 bus, as required by the FD1771-1. During output cycles, data from the processor is latched into IC33 by PWR/. During input cycles, latch IC50 is read during PDBIN.

Case 4, Output reference to port 40H: Although the data bus is not examined by the 4FDC during bank select, the data on the S-100 DO bus is latched into IC33 anyway.

Wait State Generator

The wait state generator, IC42P11, passes on wait requests when enabled by IC18. There are four enabling conditions: 1) 4MHz Inputs from ports 30-33H, 2) 4MHz M1 fetches from the ROM at C000-C3FFH, 3) Disk references with Auto Wait mode selected, and 4) Any reference to the TMS5501 (ports 00-09). There are three sources of wait request: 1) PSYNC, 2) Ready from wait IC25P8, and 3) Ready from TMS5501 (IC25P12). The coincidence of an enabling condition and a wait request stops the processor in mid cycle.

Clocks

The 4FDC has an 8.000 MHz on board crystal clock which controls all internal board timing. IC2 conditions the clock for the TMS5501 and FD1771. 2MHz 01 and 02 signals are generated at IC4P3 and IC1P10 respectively. A 1MHz timing signal is generated at IC2P15 and a switchable 2 or 1MHz clock is generated at IC2P16 (controlled by the maxi/mini signal at IC4P13).

Bank Select

The 1K ROM on board the 4FDC may be disabled through output port 40H if switch 2 (RES) is on. In this case, the ROM is deselected permanently after the first output to port 40H clocks flip-flop IC29P11 and forces IC29P9 low. This forces the memory address decoder IC30P9 high, deselecting the ROM. The ROM may be re-enabled by a hardware RESET signal which sets IC29P9 high again.

TMS5501 Interfaces

IC12 requires 12 volt clock levels at the 01 and 02 inputs. These are supplied by active pullups Q1 and Q2 which when triggered by a falling edge at the input of open collector inverter package IC25 switch on briefly to pull the inverter outputs up to 12 volts.

The serial output IC12P40 is inverted and shifted from TTL levels to +12 and -5 levels by Q3 and Q4. IC25P2 provides an open collector current sink for current loops.

The serial input IC12P5 is controlled by discrete NAND gate made up of Q5 and Q6 which shifts and inverts -5/+12 levels to +5/0 volt levels.

The parallel inputs and outputs are buffered by octal bus buffers ICs 13 and 14.

FD1771-1 Interfaces

All signals from the drives are TTL buffered and have 150 ohm pullups. Maxi and mini signals are wired and at the pullup side of the buffers. Signals which do not apply to the mini (i.e., READY and SEP CLOCK), are disabled and pulled high when the mini is selected.

Signals to the drives from the 1771 are TTL buffered with separate buffers for mini and maxi connectors. The STEP output is stretched by IC37 to about 16 microseconds before going to the drives. The HLD (head load) output does not go directly to the drives but rather enables the drive select lines through IC10P1. Thus, the actual drive select signal to the drive is the coincidence of a latched drive selection (done at port 34H) and HLD from the 1771. Head loading time is determined by counters IC36 and 27. Time-out is controlled by the count loaded into IC38 by IC53.

Signals DRQ, HLD, and INTRQ (or EOJ) are available at input port 34H (IC9). Various control signals are assigned to output port 34H and are latched by ICs 24 and 41.

Priority Chain

The 4FDC includes a ripple priority circuit which will defeat the interrupt acknowledge cycle of Priority IN/ is held low. If the 4FDC is allowed to perform the interrupt acknowledge, it will pull down its Priority Out/ line to signal others in the chain not to respond. This chain is compatible with the Cromemco TU-ART.

CHAPTER 8: PARTS LIST

4FDC Revision C

PARTS LIST

IC 1	74LS04
IC 2	74276
IC 3	74276
IC 4	74LS00
IC 5	74367
IC 6	74368
IC 7	74LS138
IC 8	74LS00
IC 9	74368
IC 10	74368
IC 11	FD 1771-1
IC 12	TMS 5501
IC 13	74LS241
IC 14	74LS240
IC 15	7905/LM320-5
IC 16	74LS04
IC 17	74LS02
IC 18	74S64
IC 19	7425
IC 20	74LS10
IC 21	74LS04
IC 22	74S260
IC 23	74903
IC 24	74LS174
IC 25	7406
IC 26	74LS04
IC 27	CD4020AE
IC 28	74LS08
IC 29	74LS74
IC 30	74S133
IC 31	2708
IC 32	74LS04
IC 33	74S373
IC 34	74LS86
IC 35	74LS86
IC 36	7420
IC 37	74164
IC 38	74161
IC 39	7812/LM340-12
IC 40	7805/LM340-5
IC 41	74LS74
IC 42	74367
IC 43	74LS03
IC 44	74L04
IC 45	74367
IC 46	74367
IC 47	74LS86
IC 48	74LS86
IC 49	74LS157
IC 50	74S373
IC 51	74LS32
IC 52	74L04
IC 53	74LS157

Transistors

Q1	2N3906
Q2	2N3906
Q3	2N3906
Q4	2N3904
Q5	2N3904
Q6	2N3904

Diodes

D1	LED, TIL-211 Green
D2	1N914
D3	1N914
D4-D6	1N4148

Resistors

R 1	1K 1/4 w
R 2	1K 1/4 w
R 3	150 1/4 w
R 4	10K 1/4 w
R 5	10K 1/4 w
R 6	10K 1/4 w
R 7	680 1/4 w
R 8	4.7K 1/4 w
R 9	1.5K 1/4 w
R10	270 1/4 w
R11	470 1/4 w
R12	4.7K 1/4 w
R13	10K 1/4 w
R14	10K 1/4 w
R15	4.7K 1/4 w
R16	4.7K 1/4 w
R17	5.6K 1/4 w
R18	390 1/4 w
R19	180 1/4 w
R20	4.7K 1/4 w
R21	330 1/4 w
R22	5.6K 1/4 w
R23	330 1/4 w

Resistors (con't)

R24	39 1/4 w
R25	39 1/4 w
R26	330 1/4 w
R27	5.6K 1/4 w
R28-29	4.7K 1/4 w

Resistor Networks

RN1	SIP, 8Pin, 7Resistors 150 ohm
RN2	SIP, 8Pin, 7Resistors 1K ohm

Capacitors

C 1	30 pF ceramic disc
C 2	10 uF tantalum
C 3	.1 uF ceramic disc
C 4	.1 uF ceramic disc
C 5	.1 uF ceramic disc
C 6	.1 uF ceramic disc
C 7	10 uF ceramic disc
C 8	10 uF ceramic disc
C 9	.1 uF ceramic disc
C10	.1 uF ceramic disc
C11	.1 uF ceramic disc
C12	.1 uF ceramic disc
C13	.1 uF ceramic disc
C14	.1 uF ceramic disc
C15	.1 uF ceramic disc
C16	.05 uF ceramic disc
C17	.1 uF ceramic disc
C18	.1 uF ceramic disc
C19	.1 uF ceramic disc
C20	.1 uF ceramic disc
C21	.05 uF ceramic disc
C22	.1 uF ceramic disc
C23	75 uF ceramic disc
C24	75 uF ceramic disc
C25	.1 uF ceramic disc
C26	.1 uF ceramic disc
C27	.1 uF ceramic disc
C28	.1 uF ceramic disc
C29	.1 uF ceramic disc
C30	.1 uF ceramic disc
C31	.05 uF ceramic disc
C32	.1 uF ceramic disc
C33	.1 uF ceramic disc
C34	.1 uF ceramic disc
C35	.1 uF ceramic disc
C36	6.8 uF tantalum
C37	10 uF tantalum

Capacitors (con't)

C38	6.8 uF tantalum
C39	.1 uF ceramic disc
C40	.1 uF ceramic disc
C41	.1 uF ceramic disc
C42	.1 uF ceramic disc
C43	.1 uF ceramic disc
C44	.1 uF ceramic disc
C45	.1 uF ceramic disc
C46	.1 uF ceramic disc
C47	.1 uF ceramic disc
C48	.1 uF ceramic disc

Miscellaneous

J2	Connector, 50Pin, Circuit Assembly, CA-D50RSP100-230-090
J3	Connector, 34Pin, Circuit Assembly, CA-D34RSP100-230-090
J4	Connector, 26Pin, Circuit Assembly, CA-D26RSP100-230-090
2	4-40 Screws and Hex Nuts
1	Heat Sink
1	8 MHz Crystal
1	4 Pole Dipswitch
5	6-32x3/8 pan head screws
5	6-32 small pattern hex nuts
1	PC board
1	Serial I/O Cable Assembly

Sockets

26	14 pin
15	16 pin
6	20 pin
1	24 pin
2	40 pin

LIMITED WARRANTY

Cromemco, Inc. warrants this 4FDC Disk Controller board against defects in materials and workmanship for a period of Ninety (90) days from the date of delivery to the customer. Cromemco, Inc. will replace or repair at its option this product should it prove to be defective due to defects in materials or workmanship during the warranty period, provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. If this product fails after the above Ninety (90) day warranty period, it will be repaired for a fixed prepaid service fee provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. Cromemco, Inc. reserves the right to refuse to repair any product that in the discretion of Cromemco, Inc. has been subjected to electrical or mechanical abuse or not handled with reasonable care. The service fee is currently $70 and is subject to change without notice.

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